IN THE CLAIMS

What is claimed is:

1. A data buffering unit, comprising:

a memory that stores data from a data transmitting device; and

a memory read manager that prepares data stored in the memory for output prior to receiving a request for the data from a data reading device.

2. The data buffering unit of Claim 1, wherein the memory comprises a plurality of first-in-first-out (FIFO) memories.

3. The data buffering unit of Claim 2, wherein the memory read manager comprises a memory enable unit that asserts a read enable line to each of the plurality of FIFO memories.

4. The data buffering unit of Claim 2, wherein the memory read manager comprises a read address manager that determines which of the plurality of FIFO memories to access in response to a read address from the data reading unit.

5. The data buffering unit of Claim 2, wherein the memory read manager comprises a read selector, coupled to data outputs of each of the FIFO memories, that selects an appropriate data output to receive data from in response to a read address from the data reading device.

6. The data buffering unit of Claim 2, wherein the memory read manager comprises a plurality of read pointer managers, each corresponding to one of the FIFO memories, the read pointer managers transmit an appropriate read address to each of the FIFO memories to prepare data to be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device.

7. The data buffering unit of Claim 2, further comprising a memory write manager that directs data from the data transmitting device to be written into each of the FIFO memories in a round robin fashion.

8. The data buffering unit of Claim 7, wherein the memory write manager comprises a write address manager that determines which of the FIFO memories to access in response to a write address received from the data transmitting device.

9. The data buffering unit of Claim 8, wherein the write address manager determines a write address in one of the FIFO memories to write data in response to the write address received from the data transmitting device.

10. The data buffering unit of Claim 7, wherein the memory write manager comprises a write selector that transmits a write enable signal and data from the data transmitting device to an appropriate FIFO memory in response to the work address manager.

11. A programmable logic device (PLD), comprising,

memory blocks that form comprises a plurality of first-in-first-out (FIFO) memories that store data from a data transmitting device; and

logic elements that form a memory read manager that prepares data stored in the FIFO memories for output prior to receiving a request for the data from a data reading device.

12. The PLD of Claim 11, wherein the memory read manager comprises a memory enable unit that asserts a read enable line to each of the plurality of FIFO memories.

13. The PLD of Claim 12, wherein the memory read manager comprises a read address manager that determines which of the plurality of FIFO memories to access in response to a read address from the data reading unit.

14. The PLD of Claim 12, wherein the memory read manager comprises a read selector, coupled to data outputs of each of the FIFO memories, that selects an appropriate data output to receive data from in response to a read address from the data reading device.

15. The PLD of Claim 12, wherein the memory read manager comprises a plurality of read pointer managers, each corresponding to one of the FIFO memories, the read pointer managers transmit an appropriate read address to each of the FIFO memories to prepare data to be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device.

16. A method for managing data, comprising:

selecting a first FIFO memory from a plurality of first-in-first-out (FIFO) memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device; and

preparing next data from a next storage element from the first FIFO memory for output.

17. The method of Claim 16, wherein the first data was prepared for output by the first FIFO memory prior to a generation of the read address from the data reading device.

18. The method of Claim 16, wherein the first data is output within a clock cycle after the first read address from the data reading device is generated.

19. The method of Claim 16, wherein preparing the next data from the next storage element from the first FIFO memory to output comprises transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.

20. The method of Claim 16, further comprising:

selecting a second FIFO memory from the plurality of FIFO memories to output second data stored in a first storage element in the second FIFO memory in response to a second read address from the data reading device; and

preparing next data from a next storage element from the second FIFO memory for output.

21. The method of Claim 20, wherein the selecting the second FIFO memory is performed during the preparing of the next data from the next storage element from the first FIFO memory for output.

22. The method of Claim 16, further comprising writing data into the plurality of FIFO memories in a round robin fashion.